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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,960	04/15/2004	Daniel J. Ferris	X-1016 US	7471

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EXAMINER	
TON, MY TRANG	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,960	FERRIS, DANIEL J.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 1, 4, 7, 10, 12-13, 16, 18 and 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the amplifier stage" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 4 (lines 4-6) is similarly rejected as claim 1.

Claim 7 recites the limitation "the supply voltage" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 is redundant recited with claim 9.

Claim 12 recites the limitations "the first transistors of the differential amplifier" in lines 4-5, "the second transistors" in line 6. There is insufficient antecedent basis for these limitations in the claim.

Claim 13 is similarly rejected as claim 12 regarding "the first transistors" in line 5 and "the second transistors" in line 7.

Claim 16 is redundant recited with claim 15.

Claim 18 recites the limitations "the differential amplifier" in lines 4 and 6 and "the load" in last line. There is insufficient antecedent basis for these limitations in the claim.

Claim 25 recites the limitation "the dual differential switching stage" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-8, 11, 14, 17-18, 20-26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Balteanu (U.S Patent No. 6,438,365).

Balteanu discloses in Fig. 3 an improved balanced mixer including:

Regarding claim 1:

a differential amplifier (Q5, Q6) for receiving and amplifying input signals (RF+, RF-), the amplifier stage (Q5, Q6) providing a predetermined gain to the input signals (RF+, RF-);

a load (Rm1, Rc1, Rc2, Rm2) for providing a load impedance;

a dual differential switching stage (Q1-Q4), coupled to the differential amplifier (Q5, Q6 via Q7-Q10) and the load (Rm1, Rc1, Rc2, Rm2), the dual differential switching stage (Q1-Q4) mixing the amplified input signals (RF+, RF-) from the differential amplifier (Q5, Q6) with a local oscillator signal (Lo+, Lo-) to produce an output signal (OUT+, OUT-) at the load (Rm1, Rc1, Rc2, Rm2); and

a current modifier (Q7-Q10), coupled to the differential amplifier (Q5, Q6), the current modifier (Q7-Q10) altering current in the differential amplifier (Q5, Q6) to adjust current through the load (Rm1, Rc1, Rc2, Rm2).

Regarding claim 3: the current modifier (Q7-Q10) comprises a current source (Q7-Q10 function as a current source), coupled to the differential amplifier (Q5-Q6), the current source (Q7-Q10) injecting current into the differential amplifier (Q5-Q6) to reduce current through the load (Rm1, Rc1, Rc2, Rm2) by supplementing current in the differential amplifier (Q5-Q6).

Regarding claim 4: the current source (Q7-Q10) comprises a first and second current device (Q7 or Q8, Q9 or Q10), the first current device (Q7 or Q8) being coupled to a first transistor (Q5) of the differential amplifier stage (Q5, Q6) and the second current device (Q9 or Q10) being coupled to a second transistor (Q6) of the differential amplifier stage (Q5, Q6).

Regarding claim 5: the current source (Q7-Q10) reduces the current flowing through the load (Rm1, Rc1, Rc2, Rm2) to enable a lower supply voltage (see col. 3, lines 22-50).

Regarding claim 6: the current source (Q7-Q10) reduces the current through the dual differential switching stage (Q1-Q4) to allow a reduction in a local oscillator drive while providing substantially the same voltage drop through the dual differential switching stage (see col. 3, lines 22-50).

Regarding claim 7: the current source (Q7-Q10) allows an increase in a voltage across the differential amplifier (Q5, Q6) while minimizing the supply voltage to provide better linearity and less distortion (col. 4, lines 27-31).

Regarding claim 8: the differential amplifier (Q5, Q6) comprises a first (Q5) and second (Q6) transistor differentially coupled having first electrodes (via Re) joined at a common node (node connected to Io1).

Regarding claim 11: the dual differential switching stage (Q1-Q4) comprises a first differential transistor pair (Q1, Q2) having first electrodes coupled at a first common connection (connected to Q8) and a second differential transistor pair (Q3, Q4) having second electrodes coupled at a second common connection (connected to Q9), the first common connection (connected to Q8) being coupled to a second electrode of the first transistor (Q5) of the differential amplifier (Q5, Q6) and the second common connection (connected to Q9) being coupled to a second electrode of the second transistor (Q6) of the differential amplifier (Q5, Q6).

Regarding claim 14: the dual differential switching stage (Q1-Q4) comprises a first differential transistor pair (Q1, Q2) having first electrodes coupled at a first common connection (connected to Q8) and a second differential transistor pair (Q3, Q4) having second electrodes coupled at a second common connection (connected to Q9).

Regarding claim 17: the dual differential switching stage (Q1-Q4) comprises first (Q1, Q2) and second (Q3, Q4) differential pairs, the first (Q1, Q2) and second (Q3, Q4) differential pairs having output electrodes cross coupled.

Claim 18 is similarly rejected as claim 1:

a Gilbert cell comprising an RF amplifier stage (Q5, Q6) and a mixer stage (Q1-Q4); and

a current modifier (Q7-Q10), coupled to the differential amplifier (Q5, Q6), the current modifier altering current in the differential amplifier (Q5, Q6) to adjust current through the load (Rm1, Rc1, Rc2, Rm2).

Claim 20 is similarly rejected as claim 3.

Claim 21 is similarly rejected as claim 4.

Claim 22 is similarly rejected as claim 5.

Claim 23 is similarly rejected as claim 6.

Claim 24 is similarly rejected as claim 7.

Claim 25 is similarly rejected as claim 17.

The method recited in claim 26 is similarly rejected as claims 1 and 18:

providing a Gilbert cell comprising an RF amplifier stage (Q5, Q6) and a mixer stage (Q1-Q4);

injecting current (Q7-Q10) into the amplifier stage (Q5, Q6) to reduce current through the mixer stage (Q1-Q4) by supplementing current in the amplifier stage (Q5, Q6).

Claim 28 is similarly rejected as claims 1, 18 and 26: means for amplifying (Q5, Q6); means for receiving (Q1-Q4); and means for injecting current (Q7-Q10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 9-10, 12-13, 15-16, 19, 27, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balteanu as applied to claims 1 and 8 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Balteanu. However, this reference does not specifically show the "current sink" (or sinking current) (claims 2, 19, 27, 29), "the first electrodes comprise sources of the first and second transistors of the differential amplifier" (claims 9-10), "the first electrodes of the first differential transistor pair comprise sources ... of the differential amplifier comprises a drain" (claims 12-13); "the first electrodes and second electrodes comprise source electrodes" (claims 15-16).

Regarding the limitation "current sink" (or sinking current) recited in claims 2, 19, 27 and 29, this appears to be obvious variations (i.e.., not patentably distinct) to limitations "a current source". Therefore, it would have been obvious to one of ordinary skill in the art to employ (the current sink), as they appear to be obvious variations (not patentably distinct) and yielding same functional device.

Regarding claim 9-10: field effect transistors (sources, drains, gates) are well-known switching devices and patentable equivalent to bipolar transistors (emitters, collectors, bases) since no unobvious results are seen produce from there use. Therefore, it would have been obvious at the time of the invention was made for one skilled in the art to utilize these particular types of transistors (FET (sources)) because of this well-known advantages in performance and integration. FETs have very short switching times and very low electrical power consumption.

Regarding claims 12-13: similarly motivation applied to claims 9-10 is applied to claims 12-13 regarding sources, drains recited therein.

Regarding claims 15-16: similarly motivation applied to claims 9-10 is applied to claims 15-16 regarding "source electrodes".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 8:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

April 26, 2005